IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Hidenori SATO et al.

Appln. No.:

Filed: Herewith

For: MANUFACTURING METHOD OF SEMICONDUCTOR INTEGRATED
    CIRCUIT DEVICE

                        *   *   *

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
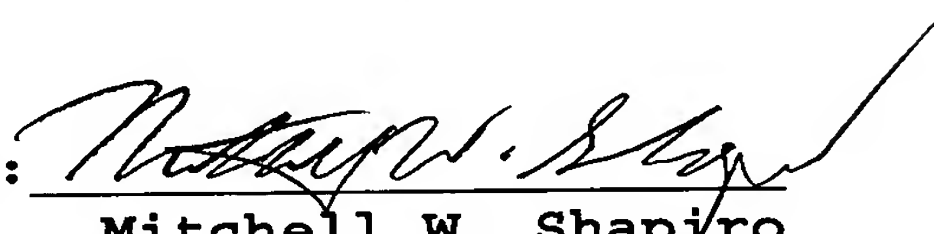P.O. Box 1450
Alexandria, VA   22313-1450

Sir:

Applicants wish to make of record the documents cited

in prior Application No. 09/905,887 filed July 17, 2001,

whether cited by Applicants or by the Patent Office.   The

documents are listed on the attached Form PTO-1449.

Respectfully submitted,

MWS:jab   By: _____
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August 19, 2003

FORM PTO-1449	Atty. Docket No.	Appln. No.
LIST OF DOCUMENTS CITED BY APPLICANT	XA-9519A	
	Applicant Hidenori SATO et al.	
	Filing Date Herewith	Group

U.S. PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Name	Class	Sub- class	Filing Date
	AA	4,489,101	12/18/84	Shibata	427	39	
	AB	4,576,678	03/18/86	Shibata	156	643	
	AC	6,235,416	05/22/01	Konig et al.	428	701	
	AD	6,118,145	09/12/00	Egawa	257	296	
	AE	6,337,272	01/08/02	Hamanaka	438	651	
	AF	6,268,295	07/31/01	Ohta et al.	438	735	
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	AI	6,337,272	01/08/02	Hamanaka	438	651	
	AJ						
	AK						

FOREIGN PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Country	Class	Sub- class	Translation
	AL	11-16999	01/22/99	Japan			Abstract
	AM	11-17147	01/22/99	Japan			Abstract
	AN	2 108 756	05/18/83	United Kingdom			No
	AO						
	AP						
	AQ						
	AR						
	AS						

OTHER (including author, title, date, pertinent pages, etc.)

	AT	

Examiner	Date Considered

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.